CERN openlab Explores New CPU/FPGA Processing Solutions

By Linda Barney

April 14, 2017

Editor's note: In this contributed feature, Linda Barney describes the ongoing technical collaboration between CERN and Intel to develop a co-packaged Xeon/FPGA processor.

At CERN, the European Organization for Nuclear Research (http://home.cern/about), physicists and engineers are probing the fundamental structure of the universe. The Large Hadron Collider (LHC), which began working in 2008, is the world's largest and most powerful particle accelerator (http://home.cern/about/how-accelerator-works); it is housed in an underground tunnel at CERN. Niko Neufeld is a deputy project leader at CERN who works on the Large Hadron Collider beauty (http://lhcb-public.web.cern.ch/lhcb-public/) (LHCb) experiment, which explores what happened after the Big Bang that allowed matter to survive and build the Universe we inhabit today.

"CERN experiments produce an enormous amount of data with forty million proton collisions every second, which leads to primary data rates of terabits per second," says Neufeld when speaking on a recent FPGA vs. CPU panel (http://www-ssl.intel.com/content/www/us/en/high-performance-computing/architecting-hpc-with-fpgas-video.html). "This is an enormous amount of data and there are a number of technical challenges in our work. We use a number of processing solutions including central processing units (CPUs), field-programmable gate arrays (FPGAs), and graphic processing units (GPUs), but each of these solutions have some limitations. We are collaborating with Intel in experimenting with a co-packaged Intel Xeon processor plus FPGA Quick Path Interconnect (QPI) processor in our LHCb research to try to determine which technology provides the best results."

CERN collaborates with leading ICT companies and other research institutes through a unique public-private partnership known as 'CERN openlab'. Its goal is to accelerate the development of cutting-edge solutions for the worldwide LHC community and wider scientific research. Through a CERN openlab project known as the 'High-Throughput Computing Collaboration,' researchers are investigating the use of various Intel technologies in data filtering and data acquisition systems.

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Figure 1. CERN researchers shown in the Large Hadron Collider tunnel in front of the LHCb detector. Courtesy of CERN (courtesty CERN).

Introducing the co-packaged Intel CPU / FPGA Processor

Today the CPU and FPGA are used as discrete chips in a solution – with an Intel Xeon processor and an FPGA which is typically attached via a PCIe interconnect to the CPU. And the development environment is also discrete using independent development tools from Intel and tools such as OpenCL and C++. Intel is working toward a common workflow and development flow to better integrate FPGAs.

"FPGA typically uses a higher level machine abstraction language (such as Verilog and VHDL) which have a painful low-level hardware programming model for most people. As a next step, Intel has a solution that co-packages the CPU and FPGA in the same Multichip Chip Product (MCP) package to deliver higher performance and lower latency than a discrete solution," states Bill Jenkins, Intel Senior AI Marketing Manager. The Intel MCP is supported by a cross-platform development framework like OpenCL that can be used to develop applications for both the CPU and FPGA. The Intel solution includes a fully unified intellectual property (IP) and development suite, including languages, libraries and development environments. The roadmap to a unified development flow leverages common tools and libraries to support both FPGA and Intel Xeon processor + FPGA systems along with an expansive ecosystem network of Intel and vendors working on independent development tools for demanding workloads such as HPC, imaging identification, security and big data.

Abstracting away FPGA Coding

Intel is building an abstraction layer (as part of the product containing the Intel CPU and FPGA in the same MCP package), called the Orchestration Software layer. This layer and the higher level IP and software models help make development less complex so that developers don't need to code specifically to the FPGA. The FPGA-enabled Orchestration software layer abstracts away the API to communicate with the FPGA as shown in the following example.

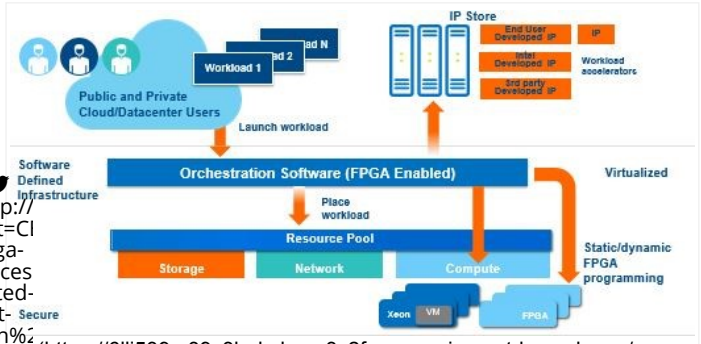

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Figure 2. Example of Intel implementation of user IP implemented into FPGA via an abstraction Orchestration software layer

There is a cloud-based library of functions and end-user IP that have been pre-compiled and built that is loaded into the FPGA at runtime. The user first launches a workload from the host and it goes into the Orchestration software which pushes a function into the FPGA. This produces a bitstream that is pre-compiled on the FPGA to bring the data in—it is almost like a fixed architecture I/O interface.

In the example scenario, users simply download the image from the abstraction Orchestration software layer to the FPGA and it is ready to run without compilation. "With the abstraction Orchestration software layer," Jenkins explained, "Intel is abstracting away all the difficulties of FPGA programming using machine language tools while enabling all the higher level Intel frameworks including the Intel Trusted Analytics Platform (TAP) and Intel Scalable System Framework (SSI) and tying the FPGA into the frameworks. Intel is developing this approach for a variety of markets including visual understanding, analytics, enterprise, Network Function Virtualization (NFV), VPN, genomics, HPC and storage."

Large Hadron Collider High-Energy Physics Research at CERN

Neufeld indicates that the experiments at CERN — through what they refer to as 'online computing' — require a first-level data-filtering to reduce the data to an amount that can be stored and processed on more traditional processing units such as Intel Xeon processors. Figure 3 shows a schematic view of the future LHCb readout system. At the top level, there is a detector and optical fiber links, which transfer data out of the detector. CERN uses FPGAs to acquire data from the detector. There are also large switching fabrics, as well as clusters of processing elements including CPUs, FPGAs, and GPUs to reduce the amount of data. One of the questions the CERN team is testing is "Which technologies should we use and which provide the best performance and lowest energy usage results?"

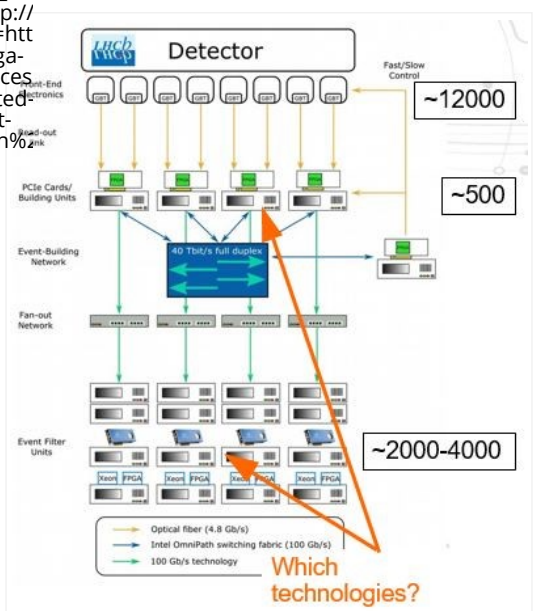

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Figure 3. Schematic diagram showing future LHCb first-level data-filtering system. Courtesy of CERN.

CERN Tests Complex Cherenkov Angle Reconstruction Calculation

CERN has extensive experience using FPGAs in their research work. “We typically use FPGAs in our research to run algorithms looking for simple integer signatures, or for other less complicated calculations. When we heard about the Intel Xeon / FPGA combined processor, we chose a test using a complex algorithm to do a Cherenkov angle reconstruction of light emission in a particle detector, which is not typically performed on an FPGA. This involves tracing a light particle — photon — through a complex arrangement of optical reflection and deflection systems. Our test case used a rich PID algorithm to calculate the Cherenkov angle for each track and detection point. This is a complex mathematical calculation that involves hyperbolic functions, roots, square roots, etc., as shown in Figure 4. It is one of the most costly calculations done in online reconstruction,” states Neufeld.

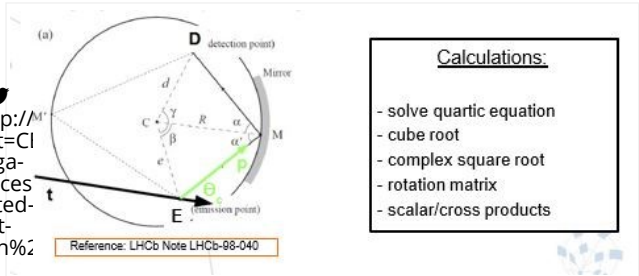

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Figure 4. Test case running Rich PID algorithm to calculate Cherenkov angle. Courtesy of CERN.

Coding the Cherenkov Angle Reconstruction in Verilog versus OpenCL

The CERN team first implemented the Cherenkov angle reconstruction by coding it in the Verilog HDL. The team wrote a 748 clock-cycle long pipeline in Verilog, along with additional blocks developed for the test including: cubic root, complex square root, rotational matrix, and cross/scalar product. It was a lengthy task doing this coding in Verilog with 3,400 lines of code. With all test benches, the implementation took 2.5 months.

Next, the team recoded the Cherenkov angle code using the OpenCL (https://en.wikipedia.org/wiki/OpenCL)and the BSP (board support package) designed to work across a variety of hardware platforms. Because OpenCL is an abstraction language, it required only 250 lines of code and took two weeks of coding. Not only was coding in OpenCL much faster but the performance results were similar. Figure 5 shows the results of the Verilog versus OpenCL implementation.

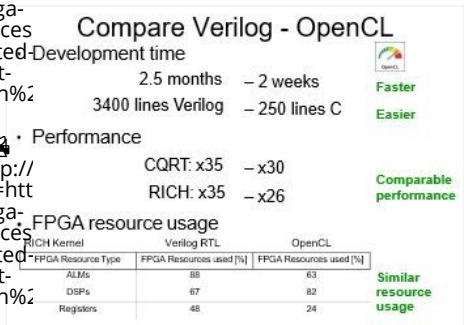

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Figure 5. Result of Verilog (CQRT) versus OpenCL (RICH) code and performance. Courtesy of CERN.

CERN Compares Co-packaged Intel Xeon – FPGA Processor against Nallatech PCIe Stratix V FPGA Board

To test performance of the Verilog code, the CERN team used a commercially available Stratix V GXA7 FPGA board / Nallatech 385 board for testing. They achieved an acceleration of a factor up to six with the Stratix – Nallatech PCIe board. However, they found a bottleneck in data transfer—they could not keep the pipeline busy because the PCIe card was limited to an eight-lane interface. Next, the CERN team did tests with the Cherenkov angle code comparing a Nallatech FPGA Board with the co-packaged Intel Xeon/FPGA QPI processor.

CERN Systems used in Test

FPGA system used by CERN	Intel/FPGA system used by CERN
Nallatech 385 board	Two socket system: • First: Intel® Xeon® E5-2680 v2
FPGA: Altera Stratix V GX A7 • 234'720 ALMs, 940'000 Registers • 256 DSPs	• Second: Intel/Altera Stratix V GX A7 FPGA ○ 234'720 ALMs, 940'000 Registers, 256 DSPs
Programming model : OpenCL	Programming model : Verilog & OpenCL
Host Interface: 8-lane PCIe Gen3 • Up to 7.5GB/s	Host Interface: • High-bandwidth and low latency
Memory: 8GB DDR3 SDRAM	Memory: Cache-coherent access to main memory
Network Enabled with (2) SFP+ 10GbE ports	

Finally, the CERN team tested an Intel Xeon CPU, PCIe Stratix V FPGA and Intel Xeon processor/Stratix V QPI (where only the interconnect was different). As shown in Figure 6, there was a factor of 9 speed up for the PCIe Stratix V FPGA and a 26 factor speed up for the Intel Xeon processor/Stratix V QPI with the faster interconnect.

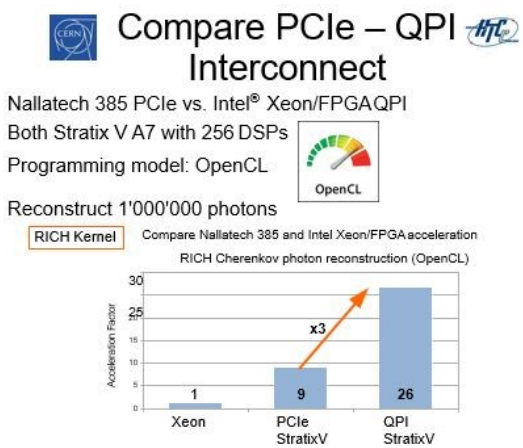

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Figure 6. Test results from the CERN team comparing Intel Xeon CPU, PCIe Stratix V FPGA and Intel Xeon processor/FPGA QPI. Courtesy of CERN.

CERN Plans to do Future Testing using co-packaged Intel Xeon/ Intel Arria10 FPGA Processor

"Our CERN team found the results of using the co-packaged Intel Xeon processor/Stratix V QPI processors to be very encouraging. In addition, we find the programming model with OpenCL attractive and it will be mandatory for the High-Energy Physics (HEP) field. Intel will be launching a co-packaged Intel Xeon processor / Intel Arria 10 FPGA processor in the future. We want to do other experiments with the co-packaged Intel Xeon processor/ Arria 10 FPGA. We expect that the high-bandwidth interconnect and modern Arria 10 FPGA card will provide high performance and performance per Joule for HEP algorithms," states Neufeld.

Linda Barney is the founder and owner of Barney and Associates, a technical/marketing writing, training and web design firm in Beaverton, OR.

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(https://www.hpcwire.com/2017/04/18/facebook-open-sources-caffe2-nvidia-intel-jumpstart-optimizations/)

From its F8 developer conference in San Jose, Calif., today, Facebook announced Caffe2, a new open-source, cross-platform framework for deep learning. Caffe2 is to Caffe, the deep learning framework developed by Berkeley AI Research and community contributors. Read more… (https://www.hpcwire.com/2017/04/18/facebook caffe2-nvidia-intel-jumpstart-optimizations/)

By Tiffany Trader

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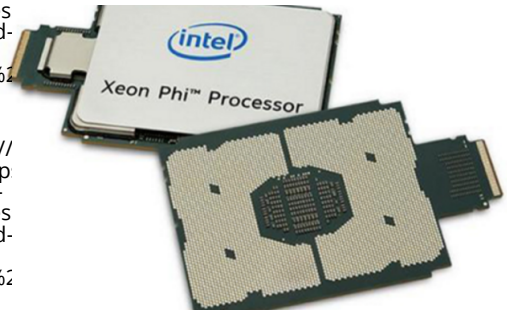

Knights Landing Processor with Omni-Path Makes Cloud Debut

(https://www.hpcwire.com/2017/04/18/knights-landing-processor-omni-path-makes-cloud-debut/)

HPC cloud specialist Rescale is partnering with Intel and HPC resource provider R Systems to offer first-ever cloud access to Xeon Phi "Knights Landing" processors. infrastructure is based on the 68-core Intel Knights Landing processor with integrated Omni-Path fabric (the 7250F Xeon Phi). Read more… (https://www.hpcwire.com/2017/04/18/knights-landing-processor-omni-path-makes-cloud-debut/)

By Tiffany Trader

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IBM Coils Anaconda Around Power Processor

(https://www.hpcwire.com/2017/04/17/ibm-coils-anaconda-around-power-processor/)

IBM, which recently extended support for the Anaconda data science platform to its open source mainframe, takes another step this week by offering the data platform Cognitive Systems platform in collaboration with Anaconda developer Continuum Analytics. Read more… (https://www.hpcwire.com/2017/04/17/ibm-coils-anaconda-a processor/)

By George Leopold

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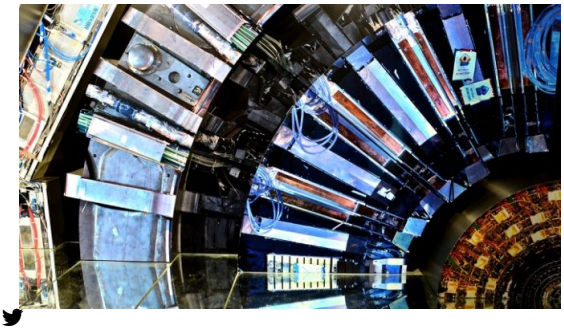

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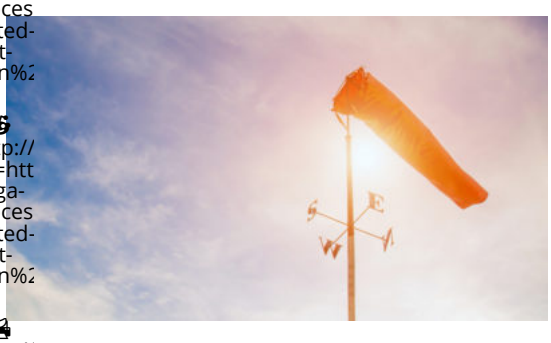
HPE Extreme Performance Solutions



HPC-Driven Weather Simulations Improving Forecasting Capabilities (https://www.hpcwire.com/solution_content/hpe/weather-climate/hpc-driven-weather-simulations-improving-forecasting-capabilities/)

In September of 1938, a massive hurricane (http://sos.ri.gov/virtualarchives/items/show/291) traversed the Atlantic Ocean and made landfall in New England. Due to i incorrect forecasting, the storm struck farther north and with greater intensity than had been predicted, leaving residents and authorities with virtually no warning or tin prepare. Read more… (https://www.hpcwire.com/solution_content/hpe/weather-climate/hpc-driven-weather-simulations-improving-forecasting-capabilities/)

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- HPE Servers Demonstrate Critical Speed for HFT Traders on STAC-N1 Test (https://www.hpcwire.com/solution_content/hpe/financial-services/hpe-servers-demonst speed-hft-traders-stac-n1-test/)

DOE Supercomputer Achieves Record 45-Qubit Quantum Simulation
(https://www.hpcwire.com/2017/04/13/doe-supercomputer-45-qubit-quantum-computer/)

In order to simulate larger and larger quantum systems and usher in an age of “quantum supremacy,” Read more… (https://www.hpcwire.com/2017/04/13/doe-superc qubit-quantum-computer/)

By Tiffany Trader

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Hyperscalers Emerging From ‘Hype Phase’

(https://www.hpcwire.com/2017/04/12/hyperscalers-emerging-hype-phase/)

The number of companies fitting the description of “hyperscale” now accounts for 68 percent of the cloud infrastructure services market, a researcher found. Read mo (https://www.hpcwire.com/2017/04/12/hyperscalers-emerging-hype-phase/)

By George Leopold

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Penguin Takes a Run at the Big Cloud Providers

(https://www.hpcwire.com/2017/04/12/penguin-takes-run-big-cloud-providers/)

HPC specialist Penguin Computing recently re-ran benchmarks from a study of its larger brethren and says the results show its ‘public cloud’ – Penguin on Demand (P among the leaders in cost and performance. Read more… (https://www.hpcwire.com/2017/04/12/penguin-takes-run-big-cloud-providers/)

By John Russell

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DDN Claims Faster Object Storage 'Cross-Region' S3 Connectivity than AWS

(https://www.hpcwire.com/2017/04/11/ddn-claims-faster-object-storage-cross-region-s3-connectivity-aws/)

Advanced-scale storage specialist DataDirect Networks (DDN), whose solutions populate the upper-rung of the Top500 supercomputing list, today announced new "cr features to its WOS object storage platform that support multi-site AWS connectivity as well as new data protection and disaster recovery capabilities. Read more… (https://www.hpcwire.com/2017/04/11/ddn-claims-faster-object-storage-cross-region-s3-connectivity-aws/)

By Doug Black

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Dutch Researchers Build Little Green Machine II Out of IBM Minsky Servers

(https://www.hpcwire.com/2017/04/11/dutch-uni-builds-little-green-machine-ii-out-of-ibm-minsky-servers/)

The newest Dutch HPC cluster is only four “pizza boxes” high, small enough to be carried around on a bicycle, but Little Green Machine II, as the new system is called research in oceanography, computer science, artificial intelligence, financial modeling and astronomy. Read more… (https://www.hpcwire.com/2017/04/11/dutch-uni-b out-of-ibm-minsky-servers/)

By Tiffany Trader

(http://twitter.com/intent/tweet?status=Dutch+Researchers+Build+Little+Green+Machine+II+Out+of+IBM+Minsky+Servers+https%3A%2F%2Fwww.hpcwire.com%2F2017%2F04%builds-little-green-machine-ii-out-of-ibm-minsky-servers%2F) (http://www.linkedin.com/shareArticle?mini=true&url=https%3A%2F%2Fwww.hpcwire.com%2F2017%2F04%2F11%2Fdutch-uni-builds-little-green-machine-ii-out-of-ibm-minsky-servers%2F&title=Dutch+Researchers+Build+Little+Green+Machine+II+Out+of+IBM+Minsky+Servers&source=https%3A%2F%2Fwww.hpcwire.con (http://www.facebook.com/sharer/sharer.php?u=https%3A%2F%2Fwww.hpcwire.com%2F2017%2F04%2F11%2Fdutch-uni-builds-little-green-machi servers%2F&title=Dutch+Researchers+Build+Little+Green+Machine+II+Out+of+IBM+Minsky+Servers/) (https://plus.google.com/share?url=https%3A%2F%2Fwww.hpcwire.com%2F2017%2F04%2F11%2Fdutch-uni-builds-little-green-machine-ii-out-of-ibm-minsky-servers%2F)

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CMU's Latest Poker Program Wins in China

(https://www.hpcwire.com/2017/04/11/cmus-latest-poker-program-wins-china/)

It's now become old hat – AI poker algorithm beats humans. Carnegie Mellon University is at the forefront of creating this new class of crafty AI gamblers. Read more. (https://www.hpcwire.com/2017/04/11/cmus-latest-poker-program-wins-china/)

By John Russell

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